AMENDMENTS TO THE CLAIMS:

Please cancel Claims 1-16 without prejudice or disclaimer of the subject matter presented therein.

Please add new Claims 17-22 as follows. In accordance with the revised amendment format, all claims are presented below.

1-16 (Cancelled)

17. (New) A sensor chip formed on a single semiconductor chip, comprising:

an image pickup portion which includes a plurality of photoelectric conversion elements;

a scan circuit which reads out a signal from said image pickup portion;

a drive pulse generation circuit which generates a drive pulse for driving said scan circuit;

a reference clock signal generation circuit which generates a first reference clock signal;

a terminal which inputs a second reference clock signal from outside said sensor chip; and

a switch which effects switching so that said drive pulse generation circuit generates the drive pulse for said scan circuit on the basis of one of the first reference clock signal and the second reference clock signal.

18. (New) A sensor chip according to claim 17, wherein said drive pulse generation circuit generates a first pulse for driving said scan circuit so as to read out the signal from said image pickup portion in a first mode, and a second pulse for driving said scan circuit so as to read out the signal from said image pickup portion in a second mode, and wherein said sensor chip further comprises a first control circuit which effects control so that said drive pulse generation circuit generates the first pulse, and a terminal which inputs a control signal from outside said semiconductor chip for controlling said drive pulse generation circuit so as to generate the second pulse.

19. (New) A sensor chip according to claim 18, wherein the first mode is a mode for reading out the signal from said image pickup portion at a resolution lower than that of the second mode.

20. (New) A drive pulse generation chip formed on a single semiconductor chip, comprising:

a drive pulse generation circuit which generates a drive pulse;

a reference clock signal generation circuit which generates a first reference clock signal;

a terminal which inputs a second reference clock signal from the external of said drive pulse generation chip; and

a switch which effects switching so that said drive pulse generation circuit generates the drive pulse on the basis of one of the first reference clock signal and the second reference clock signal.

21. (New) A drive pulse generation chip according to claim 20, wherein said drive pulse generation circuit generates a first pulse for a first drive mode and a second pulse for a second drive mode, and

wherein said drive pulse generation chip further comprises a first control circuit which effects control so that said drive pulse generation circuit generates the first pulse, and a terminal which inputs a control signal from outside said drive pulse generation chip for controlling said drive pulse generation circuit so as to generate the second pulse.

22. (New) An image pickup apparatus comprising:

a sensor chip formed on a single semiconductor substrate,

said sensor chip comprising:

an image pickup portion which includes a plurality of photoelectric conversion elements;

a scan circuit which reads out a signal from said image pickup portion;

a drive pulse generation circuit which generates a drive pulse for driving said scan circuit, said drive pulse generation circuit generating a first pulse for driving said scan circuit so as to read out the signal from said image pickup portion in a first mode, and a second pulse for driving said scan circuit so as to read out the signal from said image pickup portion in a second mode;

a reference clock signal generation circuit which generates a first reference clock signal;

a terminal which inputs a second reference clock signal from outside

said semiconductor substrate;

a switch which effects switching so that said drive pulse generation circuit generates the drive pulse of said scan circuit on the basis of one of the first reference clock signal and the second reference clock signal; and

a first control circuit which effects control so that said drive pulse generation circuit generates the first pulse,

said image pickup apparatus further comprising a second control circuit which is provided externally to said semiconductor substrate and effects control so that said drive pulse generation circuit generates the second pulse.